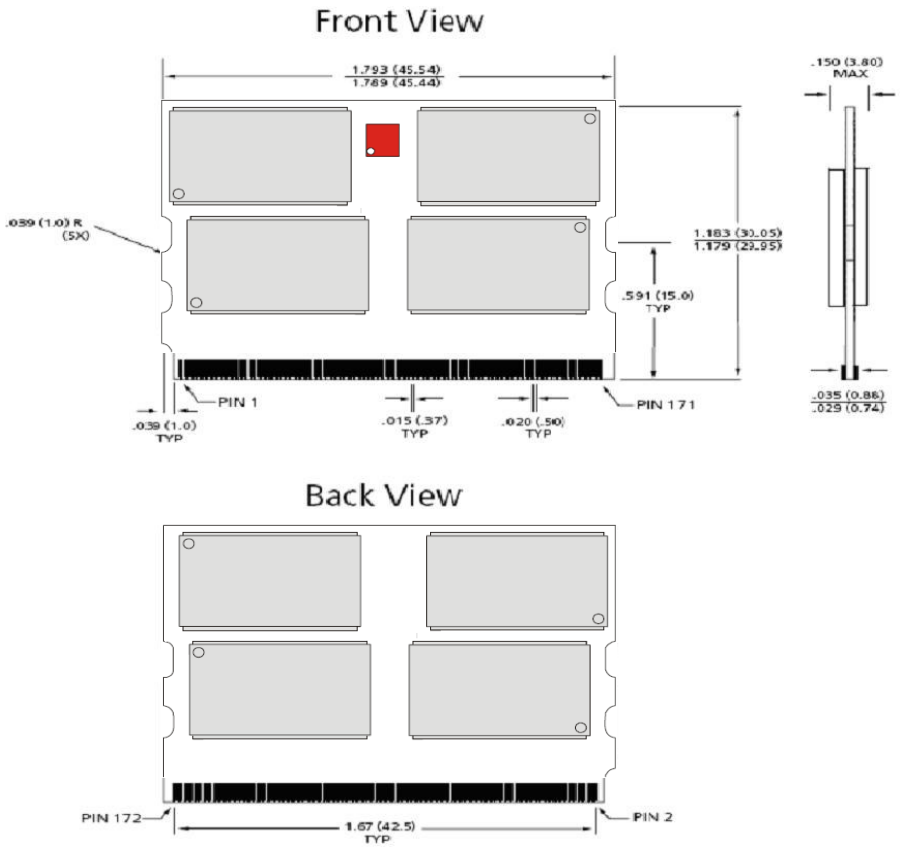
1. Features

- **Fast data transfer rates: PC2-4200**
- **172-pin, Dual In-Line Memory module**
- **VDD = VDDQ = +1.8V, VDDSPD = +1.7V to +3.6V**
- **JEDEC standard_1.8V I/O (SSTL_1.8-compatible)**
- **Differential data strobe (DQS, /DQS) option**
- **Four-bit prefetch architecture**
- **DLL to align DQ and DQS transitions with CK**
- **Multiple internal device banks for concurrent operation**
- **Programmable /CAS latency (CL)**
- **Posted /CAS additive latency (AL)**
- **WRITE latency = READ latency - 1 tCK**
- **Programmable burst lengths: 4 or 8**
- **Adjustable data-output drive strength**
- **64ms, 8,192-cycle refresh**
- **On-die termination (ODT)**
- **92ball FBGA Leaded & Pb-Free (RoHS compliant) package**

2. Module Specification

Item	Specification
Capacity	1024MByte
Physical Bank(s)	1
Module Organization	128M x 64bit
Module Type	nonECC
Speed Grade	PC2-4200 (DDR2 533)
Voltage Interface	SSTL_18
Power Supply Voltage	1.8V ± 0.1V
Burst Lengths	4 or 8
DRAM Organization	128M x 8bit DDR2 SDRAM
PCB Layer	6Layers
Contact Tab	172 pin GOLD Flash Plating
Serial PD	Support

3. Simplified Mechanical Drawing with Keying Positions



Notes： 1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.

4. Pinouts

Pin Num	Pin Name	Pin Num	Pin Name	Pin Num	Pin Name	Pin Num	Pin Name	Pin Num	Pin Name	Pin Num	Pin Name
1	VREF	61	DQS3	121	DQS5	2	VREF	62	DM3	122	DM5
3	VSS	63	VSS	123	VSS	4	VSS	64	VSS	124	VSS
5	DQ0	65	DQ26	125	DQ42	6	DQ4	66	DQ30	126	DQ46
7	DQ1	67	DQ27	127	DQ43	8	DQ5	68	DQ31	128	DQ47
9	VDD	69	VDD	129	VDD	10	VDD	70	VDD	130	VDD
11	DQS0	71	DNU	131	VDD	12	DM0	72	CKE0	132	/CK1
13	DQ2	73	A12	133	VSS	14	DQ6	74	A11	134	CK1
15	VSS	75	A9	135	VSS	16	VSS	76	A8	136	VSS
17	DQ3	77	A7	137	DQ48	18	DQ7	78	A6	138	DQ52
19	DQ8	79	VSS	139	DQ49	20	DQ12	80	VSS	140	DQ53
21	VDD	81	A5	141	VDD	22	VDD	82	A4	142	VDD
23	DQ9	83	A3	143	DQS6	24	DQ13	84	A2	144	DM6
25	DQS1	85	A1	145	DQ50	26	DM1	86	A0	146	DQ54
27	VSS	87	A10/AP	147	VSS	28	VSS	88	BA1	148	VSS
29	DQ10	89	VDD	149	DQ51	30	DQ14	90	VDD	150	DQ55
31	DQ11	91	BA0	151	DQ56	32	DQ15	92	/RAS	152	DQ60
33	VDD	93	/WE	153	VDD	34	VDD	94	/CAS	154	VDD
35	CK0	95	/S0	155	DQ57	36	VDD	96	DNU	156	DQ61
37	/CK0	97	NC	157	DQS7	38	VSS	98	NC	158	DM7
39	VSS	99	VSS	159	VSS	40	VSS	100	VSS	160	VSS
41	DQ16	101	DQ32	161	DQ58	42	DQ20	102	DQ36	162	DQ62
43	DQ17	103	DQ33	163	DQ59	44	DQ22	104	DQ37	164	DQ63
45	VDD	105	VDD	165	VDD	46	VDD	106	VDD	166	VDD
47	DQS2	107	DQS4	167	SDA	48	DM2	108	DM4	168	SA0
49	DQ18	109	DQ34	169	SCL	50	DQ22	110	DQ38	170	SA1
51	VSS	111	VSS	171	VDDSPD	52	VSS	112	VSS	172	SA2
53	DQ19	113	DQ35			54	DQ23	114	DQ39		
55	DQ24	115	DQ40			56	DQ28	116	DQ44		
57	VDD	117	VDD			58	VDD	118	VSS		
59	DQ25	119	DQ41			60	DQ29	120	DQ45		

5. Pin Description

SYMBOL	TYPE	DESCRIPTION
CK, /CK	Input	**Clock:** CK and /CK are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of /CK. Output data (DQs and DQS /DQS) is referenced to the crossings of CK and /CK.
/RAS, /CAS, /WE	Input	**Command Inputs:** /RAS, /CAS and /WE (along with /S) define the command being entered.
CKE	Input	**Clock Enable:** CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for power down entry and exit, and for self refresh entry. CKE is asynchronous for self refresh exit. CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, CK, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during self refresh.
/S0-/S1	Input	**Chip Select:** Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. Rank 0 is selected by S0; Rank 1 is selected by S1
DM0-DM7	Input	**Input Data Mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. For x8 device, the function of DM or RDQS/RDQS is enabled by EMRS command.
BA0 – BA1	Input	**Bank Address Inputs:** BA0 and BA1 for 256 and 512Mb, BA0 - BA2 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines if the mode register or extended mode register is to be accessed during a MRS or EMRS cycle.
A0 - A12	Input	**Address Inputs:** Provided the row address for Active commands and the column address and Auto Precharge bit for Read/Write commands, to select one location out of the memory array in the respective bank. A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1. The address inputs also provide the op-code during Mode Register Set commands.
DQ0-DQ63	Input/Output	**Data bit Input/ Output:** Bi-directional data bus.
DQS0-DQS7	Input/Output	**Data Strobe:** output with read data, input with write data for source-synchronous operation. Edge-aligned with read data, center-aligned with write data. For Rawcards using x16 orginized DRAMs DQ0-7 connect to the LDQS pin of the DRAMs and DQ8-17 connect to the UDQS pin of the DRAM.
NC		**No Connect:** No internal electrical connection is present.
DNU		Do net use
V_{DD}, V_{SS}	Supply	Power and ground for the DDR2 SDRAM input buffers, and core logic. V_{DD} and V_{DDQ} pins are tied to V_{DD} / V_{DDQ} planes on these modules.
V_{REF}	Supply	Reference voltage for SSTL 18 inputs.
SDA	Input/Output	This bidirectional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to V_{DD} to act as a pullup on the system board.
SCL	Input	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus time to V_{DD} to act as a pullup onthe system board.
V_{DD}SPD	Supply	Power supply for SPD EEPROM. This supply is separate from the V_{DD} / V_{DDQ} power plane. EEPROM supply is operable from 1.7V to 3.6V.
SA0-SA2	Input	These signals and tied at the system planar to either VSS or VDD to configure the serial SPD EERPOM address range.